Stevenson #3 2-12-01

JAN 18 2001

Attorney Docket No. 18940/36899
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Matsumoto Toshiyuki, Yakabe Masami, Hirota Yoshihiro		
Serial No.:	09/703,845	Group:	2858
Filed:	November 2, 2000	Examiner:	

For: CAPACITANCE MEASUREMENT METHOD OF MICRO STRUCTURES OF INTEGRATED CIRCUITS

SUBMISSION UNDER 37 C.F.R. 1.56, 1.97 & 1.98
INFORMATION DISCLOSURE STATEMENT

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

To comply with the duty of disclosure set forth in 37 CFR 1.56, the prior art listed on the attached PTO-1449 is submitted herewith to the Examiner for consideration in connection with the examination of the above-identified application.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 02-1010 (18940/36899).

Respectfully submitted,

BARNES & THORNBURG

JAN 18 2001

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JAN 18 2001

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY DOCKET NO.	SERIAL NO.
18940/36899	09/703,845
APPLICANT	
M. Toshiyuki, Y. Masami, H. Yoshihiro	
FILING DATE	GROUP
November 2, 2000	2858

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	3,753,373	8/21/1973	Brown			
	AB	4,473,796	9/25/1984	Nankivil			
	AC	4,498,044	2/5/1985	Horn			
	AD	5,416,470	5/16/1995	Tanaka et al.			
	AE	5,701,101	12/23/1997	Weinhardt et al.			
	AF	5,808,516	9/15/1998	Barber			
	AG	5,886,529	3/23/1999	Wakamatsu			
	AH	5,986,456	11/16/1999	Yamashita			
	AI	6,054,867	4/25/2000	Wakamatsu			
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION Yes	TRANSLATION No
	AL	3413849 A1	8/22/1985	Germany				
	AM	61-14578	1/22/1986	Japan				
	AN	06180336	6/28/1994	Japan (Abstract)				
	AO	4135991 C1	12/17/1992	Germany				
	AP	9-280806	10/31/1997	Japan				

OTHER PRIOR ART *(Including Author, Title, Date Pertinent Pages, Etc.)*

	AQ		*An On-Chip, Attofarad Interconnect Charge-Based Capacitance Measurement (CBCM Technique)*, J.C. Chen, B.W. McGaughy, D. Sylvester, C. Hu, Department of EECS, University of California Berkeley, 1996
	AR		*On-Chip Measurement of Interconnect Capacitances in a CMOS Process*, A. Khalkhal and P. Nouet, Laboratoire d'Informatique, de Robotique et de Microelectronique de Montpellier (LIRMM), Proc. IEEE 1995 Int. Conference on Microelectroic Test Structures, Vol. 8, March, 1995
	AS		*Efficient extraction of metal parasitic capacitances*, G.J. Gaston and I.G. Daniels, GEC Plessey Semiconductors Ltd., Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures, Vol. 8, March, 1995

SM	AT		*Op-amp circuit measures diode-junction capacitance*, by D. Monticelli and T. Frederiksen, Engineer's notebook, Electronics, July 10, 1975

EXAMINER: T.R. Lund DATE CONSIDERED: 5/22/02

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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